**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An electronic device to process digital data belonging to a set of $2^n$ codes in which a relation of order is established and in which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a conversion circuit for said digital data to be processed and adapted to reduce processing time of a high volume of said data by a computer, by generation of a transform that is a binary number having $2^n$-1 binary elements T[x] with x = 1 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[2]\ T[1]$$

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

circuits to receive a result of the conversion circuit and to carry out a digital processing of said result,

wherein an original code of the digital data to be processed includes a signed type,

wherein said conversion circuit is integrated in a semiconductor circuit so as to enable said transform to be performed within said semiconductor circuit to increase data processing speed, and

wherein said conversion circuit is adapted to produce higher processing timesaving as a number of said digital data to be processed gets larger.

2. (Currently Amended) An electronic device to process digital data belonging to a set of $2^n$ codes in which a relation of order is established and in which each of said data has a rank R between 0 and $2^n$-1, the device comprising:

a conversion circuit for said digital data to be processed and adapted to reduce processing time of a high volume of said data by a computer, by generation of a transform that is a binary number having $2^n$ binary elements T[x] with x = 0 to $2^n$-1:

$$T[2^n-1]\ T[2^{n-}2]\ \ldots T[x]\ldots\ T[1]\ T[0]$$

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

circuits to receive a result of the conversion circuit and to carry out a digital processing of said result

wherein an original code of the digital data to be processed includes a signed type,

wherein said conversion circuit is integrated in a semiconductor circuit so as to enable said transform to be performed within said semiconductor circuit to increase data processing speed, and

wherein said conversion circuit is adapted to produce higher processing timesaving as a number of said digital data to be processed gets larger.

3. (Previously Presented) The device according to claim 1 wherein said digital processing includes a Boolean OR carried out in bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a maximum value of a set of digital values.

4. (Previously Presented) The device according to claim 3 wherein the read out of said maximum value is followed by a comparison with another value.

5. (Previously Presented) The device according to claim 2 wherein said digital processing includes a Boolean AND, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a minimum value of a set of digital values.

6. (Previously Presented) The device according to claim 5 wherein the read out of said minimum value is followed by a comparison with another value.

7. (Currently Amended) An electronic device to process digital data belonging to a set of $2^n$ codes in which a relation of order is established and in which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

–a conversion circuit for said digital data to be processed and adapted to reduce processing time of a high volume of said data by a computer, by generation of a transform that is a binary number having $2^n$-1 binary elements T[x] with x = 1 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[2]\ T[1]$$

wherein T(x) = 1 when x is strictly higher than R and T(x) = 0 when x is lower or equal to R; and

circuits to receive a result of the conversion circuit and to carry out a digital processing of said result,

wherein an original code of the digital data to be processed includes a signed type,

wherein said conversion circuit is integrated in a semiconductor circuit so as to enable said transform to be performed within said semiconductor circuit to increase data processing speed, and

wherein said conversion circuit is adapted to produce higher processing timesaving as a number of said digital data to be processed gets larger.

8. (Currently Amended) An electronic device to process digital data belonging to a set of $2^n$ codes in which a relation of order is established and in which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a conversion circuit for each digital data to be processed and adapted to reduce processing time of a high volume of said data by a computer, by generation of a transform that is a binary number having $2^n$ binary elements T[x] with x = 0 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[1]\ T[0]$$

wherein T(x) = 1 when x is strictly higher than R and T(x) = 0 when x is lower or equal to R; and

circuits to receive a result of the conversion circuit and to carry out a digital processing of said result,

wherein an original code of the digital data to be processed includes a signed type,

wherein said conversion circuit is integrated in a semiconductor circuit so as to enable said transform to be performed within said semiconductor circuit to increase data processing speed, and

wherein said conversion circuit is adapted to produce higher processing timesaving as a number of said digital data to be processed gets larger.

9. (Previously Presented) The device according to claim 7 wherein said digital processing includes a Boolean AND, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a maximum value of a set of digital values.

10. (Previously Presented) The device according to claim 9 wherein the read out of said maximum value is followed by a comparison with another value.

11. (Previously Presented) The device according to claim 8 wherein said digital processing includes a Boolean OR, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a minimum value of a set of digital values.

12. (Previously Presented) The device according to claim 11 wherein the read out of said minimum value is followed by a comparison with another value.

13. (Previously Presented) The device according to claim 8 wherein the original code of the digital data to be processed further includes an unsigned type, Gray, Johnson, and includes a mantissa and an exponent.

14. (Previously Presented) The device according to claim 7 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

15. (Currently Amended) An electronic device to read out a maximum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$-1 binary elements T[x] with x = 1 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[2]\ T[1]$$

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

logic circuits to carry out a logical OR in a bit-serial way on bits of same index of said digital data, in order to read out the maximum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

16. (Currently Amended) An electronic device to read out a maximum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$ binary elements T[x] with x = 0 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[1]\ T[0]$$

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

logic circuits to carry out a logical OR in a bit-serial way on bits of same index of said digital data, in order to read out the maximum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

17. (Currently Amended) An electronic device to read out a minimum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$ -1 binary elements T[x] with x = 1 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[2]\ T[1]$$

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

logic circuits to carry out a logical AND in a bit-serial way on bits of same index of said digital data, in order to read out the minimum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

18. (Currently Amended) An electronic device to read out a minimum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$ binary elements T[x] with x = 0 to $2^n$-1:

$$T[2^n-1]\ T[2^n-2]\ \ldots T[x]\ldots\ T[1]\ T[0]$$

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

logic circuits to carry out a logical AND in a bit-serial way on bits of same index of said digital data, in order to read out the minimum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

19. (Currently Amended) An electronic device to read out a maximum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$ -1 binary elements T[x] with x =1 to $2^n$-1:

$$T[2^n-1]\ T[2^n-2]\ \ldots T[x]\ldots\ T[2]\ T[1]$$

wherein T(x) = 1 when x is strictly higher than R and T(x) = 0 when x is lower or equal to R; and

logic circuits to carry out a logical AND in a bit-serial way on bits of same index of said digital data, in order to read out the maximum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

20. (Currently Amended) An electronic device to read out a maximum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$ binary elements T[x] with x =0 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[1]\ T[0]$$

wherein T(x) = 1 when x is strictly higher than R and T(x) = 0 when x is lower or equal to R; and

logic circuits to carry out a logical AND in a bit-serial way on bits of same index of said digital data, in order to read out the maximum of said set of digital data,

wherein an original code of the data includes a signed type, and

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

21. (Currently Amended) An electronic device to read out a minimum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$-1 binary elements T[x] with x = 1 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[2]\ T[1]$$

wherein T(x) = 1 when x is strictly higher than R and T(x) = 0 when x is lower or equal to R; and

logic circuits to carry out a logical OR in a bit-serial way on bits of same index of said digital data, in order to read out the minimum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

22. (Currently Amended) An electronic device to read out a minimum among a set of digital data belonging to a set of $2^n$ codes in which a relation of order is established and for which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a circuit adapted to reduce processing time of a high volume of said data by a computer, by being adapted to represent each one of said digital data as a code having $2^n$ binary elements T[x] with x = 0 to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[1]\ T[0]$$

wherein T(x) = 1 when x is strictly higher than R and T(x) = 0 when x is lower or equal to R; and

logic circuits to carry out a logical OR in a bit-serial way on bits of same index of said digital data, in order to read out the minimum of said set of digital data,

wherein an original code of the data includes a signed type,

wherein said circuit to reduce processing time is integrated in a semiconductor circuit so as to enable transformations into said T[x] to be performed within said semiconductor circuit to increase data processing speed, and

wherein said circuit to reduce processing time is adapted to produce higher processing timesaving as a number of said data gets larger.

23. (Currently Amended) An electronic apparatus, comprising:

a conversion circuit to receive digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank, the conversion circuit being capable to reduce processing time of a high volume of said data by a computer, by being adapted to transform the received digital data into a binary number having binary elements

whose values are based at least in part on a value of the rank, wherein an original code of the digital data to be processed includes a signed type; and

a processing circuit coupled to the conversion circuit to receive the digital data that has been transformed to the binary number and to generate a result therefrom,

wherein said conversion circuit is integrated in a semiconductor circuit so as to enable said transform to be performed within said semiconductor circuit to increase data processing speed, and

wherein said conversion circuit is adapted to produce higher processing timesaving as a number of said data gets larger.

24. (Original) The apparatus of claim 23 wherein the conversion circuit includes a plurality of conversion units, each being capable to transform their respective digital data from the set into a binary number.

25. (Original) The apparatus of claim 23 wherein the processing circuit includes:

a first unit coupled to the conversion circuit to apply a logical operation on binary numbers received from the conversion circuit to generate at least one output therefrom; and

a second unit coupled to the first unit to perform a reverse transform on the at least one output from the first unit to generate the result.

26. (Original) The apparatus of claim 25 wherein the logical operation comprises a logical OR operation carried out in a bit-serial manner on bits of the binary numbers of same index.

27. (Previously Presented) The apparatus of claim 25 wherein the logical operation includes a logical AND operation carried out in a bit-serial manner on bits of the binary numbers of same index.

28. (Original) The apparatus of claim 23 wherein the result includes a minimum value of the set of digital data.

29. (Original) The apparatus of claim 23 wherein the result includes a maximum value of the set of digital data.

30. (Original) The apparatus of claim 23, further comprising at least another circuit coupled to the processing circuit to compare the result with another value.

31. (Currently Amended) A method of operating an electronic device, the method comprising:

receiving digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank, wherein an original code of the digital data includes a signed type;

reducing processing time of a high volume of said data by a computer, by transforming each of the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank; and

processing the digital data that has been transformed into the binary numbers to generate a result therefrom,

wherein said electronic device is integrated in a semiconductor circuit so as to enable said transforming to be performed within said semiconductor circuit to increase data processing speed, and

wherein said reducing processing time produces higher processing timesaving as a number of said data gets larger.

32. (Original) The method of claim 31 wherein processing the digital data that has been transformed into the binary numbers includes:

applying a logical operation on the binary numbers to generate at least one output therefrom; and

performing a reverse transform on the at least one output to generate the result.

33. (Original) The method of claim 32 wherein applying the logical operation includes applying a logical OR operation in a bit-serial manner on bits of the binary numbers of same index.

34. (Original) The method of claim 32 wherein applying the logical operation includes applying a logical AND operation in a bit-serial manner on bits of the binary numbers of same index.

35. (Original) The method of claim 31 wherein generating the result includes at least one of generating a maximum and a minimum value of the set of digital data.

36. (Original) The method of claim 31, further comprising comparing the generated result with another value.

37. (Currently Amended) An electronic apparatus, comprising:

a means for receiving digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank;

a means for reducing processing time of a high volume of said data by a computer, by transforming each of the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank, wherein an original code of the digital data includes a signed type; and

a means for processing the digital data that has been transformed into the binary numbers to generate a result therefrom,

wherein said means for reducing processing time is integrated in a semiconductor circuit so as to enable said transforming to be performed within said semiconductor circuit to increase data processing speed, and

wherein said means for reducing processing time produces higher processing timesaving as a number of said data gets larger.

38. (Original) The apparatus of claim 37 wherein the means for processing the digital data that has been transformed into the binary numbers includes:

a means for applying a logical operation on the binary numbers to generate at least one output therefrom; and

a means for performing a reverse transform on the at least one output to generate the result.

39. (Original) The apparatus of claim 38 wherein the means for applying the logical operation includes at least one of a means for applying a logical OR operation and a logical AND operation in a bit-serial manner on bits of the binary numbers of same index.

40. (Original) The apparatus of claim 38 wherein the means for processing the digital data to generate the result includes at least one of a means for generating a maximum and a minimum value of the set of digital data.

41. (Original) The apparatus of claim 38, further comprising a means for comparing the generated result with another value.

42. (Previously Presented) The device according to claim 2 wherein said digital processing includes a Boolean OR, carried out in bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out the maximum value of a set of digital values.

43. (Previously Presented) The device according to claim 1 wherein said digital processing includes a Boolean AND, carried out in a bit-serial way on bits of same index

of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a minimum value of a set of digital values.

44. (Previously Presented) The device according to claim 8 wherein said digital processing includes a Boolean AND, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a maximum value of a set of digital values.

45. (Previously Presented) The device according to claim 7 wherein said digital processing includes a Boolean OR, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of said transform, in order to read out a minimum value of a set of digital values.

46. (Previously Presented) The device according to claim 15 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

47. (Previously Presented) The device according to claim 16 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

48. (Previously Presented) The device according to claim 17 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

49. (Previously Presented) The device according to claim 18 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

50. (Previously Presented) The device according to claim 19 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

51. (Previously Presented) The device according to claim 20 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

52. (Previously Presented) The device according to claim 21 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

53. (Previously Presented) The device according to claim 22 wherein said transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data.

54. (Currently Amended) An electronic device to process digital data belonging to a set of $2^n$ codes in which a relation of order is established and in which each of said data has a rank R between 0 and $2^n$-1, said device comprising:

a conversion circuit for said digital data to be processed and adapted to reduce processing time of a high volume of said data by a computer, by generation of a transform that is a binary number having $2^n$-1 binary elements T[x] with x = a to $2^n$-1:

$$T[2^n\text{-}1]\ T[2^n\text{-}2]\ \ldots T[x]\ldots\ T[b]$$

with a and b being equal to 0 or 1,

wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R; and

circuits to receive a result of the conversion circuit and to carry out a digital processing of said result,

wherein an original code of the digital data to be processed includes a signed type,

wherein said conversion circuit is integrated in a semiconductor circuit so as to enable said transform to be performed within said semiconductor circuit to increase data processing speed, and

wherein said conversion circuit is adapted to produce higher processing timesaving as a number of said data to be processed gets larger.

55. (Previously Presented) The device according to claim 54 wherein (a,b) is equal to (1,1).

56. (Previously Presented) The device according to claim 54 wherein (a,b) is equal to (0,0).

57. (Previously Presented) The device according to claim 54 wherein (a,b) is equal to (0,1).

58. (Previously Presented) The device according to claim 54 wherein (a,b) is equal to (1, 0).

59. (New) The device of claim 1 wherein said conversion circuit is adapted to simultaneously carry out each of said transform of said data.